80437FX System Controller (TSC) and 82438FX Data Path unit (TDP), Intel Corp., pp 1-67, 11/96 (INTEL). The Applicant respectfully traverses the Examiner's rejection.

The Office Action, under MPEP §§ 2124 and 2131.01, attempts to combine EN with INTEL, which has a publication date after the filing date of the present application, to reject the pending claims. The Office Action states, in short, that EN "discloses the invention as claimed. EN discloses [the] Triton PCI Chip set.", and that INTEL shows " inherent" characteristics (i.e., first and second memory devices are page mode memory and Burst EDO memory) not specifically disclosed in EN.

MPEP §2112 sets forth the standard for reliance on inherency to reject claims. It requires the Examiner to provide rationale or evidence tending to show such inherency in accordance with the following two standards.

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir 1993) (emphasis added).
>
> In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the inherent characteristic necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter., 1990) (emphasis in original).

The Applicant respectfully asserts that the Examiner has not met the above standards for the reasons set forth below. EN merely discloses the existence of the Triton chip set. EN does not disclose burst mode memory, while each one of the currently pending claims specifically includes the element of "burst EDO" memory.

While the device discussed in EN may operate using the EDO mode or Page mode, there is no evidence that the device disclosed by EN will operate with burst mode memories. Accordingly, under the guidance of MPEP §2112, EN is not determinative of inherency with respect to burst mode memory operation.

Further, reliance on INTEL to confirm burst mode memory operation of the device disclosed by EN is misplaced. INTEL does not teach burst mode operation, merely determining whether memory is EDO or Page mode, as evidenced by a single bit being set based on the determination. While INTEL does use the term "burst" on page 45, it does not teach burst write operations.

Moreover, since INTEL is dated well after the priority filing date of the instant application, using Intel to read into EN that which is not inherent within EN is improper. INTEL does not teach, or even suggest, burst writes. Consequently, INTEL can not be used to read into EN that which INTEL does not teach.

Finally, the Applicant requests identification by the Examiner of specific sections in INTEL which support the rejection. The Applicant's understanding of the INTEL reference disagrees with the interpretation set forth in the Office Action. For example, the Office Action states that page 45 of the INTEL reference supports inherency of Burst EDO memory. However, the Applicant notes that the algorithm discussed on page 45 of the INTEL reference requires an EDO Detect Mode Enable bit in the DRAMC register be set to enable a special timing mode for BIOS to detect the DRAM type on a row by row basis. *See*, INTEL, §4.4.5, second paragraph, and §4.4.5.1(2), second bullet. The special timing mode enabled in the INTEL algorithm suggests that reading data from the memory does not occur in a standard EDO burst mode.

In view of the foregoing, Applicant respectfully requests withdrawal of the rejection of claims 26, 29, 32, and 35-39 under 35 U.S.C. §102(a).

§103 Rejection of the Claims

Claims 27-28, 30-31, 33 and 34 were rejected under 35 USC § 103(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset Datasheet 82437FX System Controller (TSC) and 82438FX Data Path Unit (TDP), Intel Corp., pp. 1-67, 11/96 (INTEL) and further in view of Fung et al. (Fung) US Patent No. 5,630,163. The Applicant respectfully traverses the Examiner's rejection of these claims.

The Examiner notes that EN and INTEL fail to disclose a power supply, or a power up detection circuit ... to cause the processor to detect the memory device mode and to program the

memory controller, as claimed by the Applicant. The Examiner goes on to assert that Fung discloses a "power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (Col. 1, lines 25-32)." However, quoting from the cited portion of Fung, the Applicant finds the following: "The system service routines provide program loading, memory size determination, ..., and other system services." The Applicant fails to find where Fung teaches or even suggests detecting the memory device mode; Fung merely speaks to determining the memory *size.* This being the case, the Applicant respectfully requests specific citation to the text of Fung which speaks to detecting the memory device mode of operation.

Claims 26, 29, 32 and 35-39 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al (Farrer) US Patent No. 5,307,320 in view of Micron, "Ruduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and further in view of Wyland US Patent No. 5,261,064. The Applicant respectfully traverses the Examiner's rejection of these claims.

After noting that Farrer fails to disclose several elements of the present invention, the Examiner asserts that combining the Micron reference to supply some of the missing elements would be "obvious to one having ordinary skill in the art at the time the invention was made ... for the advantages stated above." However, this conclusion based on the cited combination of references is improper.

The Examiner appears to rely on official notice of facts outside the record to support the deficiency noted in the references. This improper reliance is even more obvious when considering the assertion by the Examiner that, while neither Farrer nor Micron disclose a burst mode of operation, as recited in every claim by the Applicant, "it is well known in the memory art [that] a memory can be operate[d] in a burst mode. For example Wyland discloses [a] burst mode of operation ..." The Applicant disagrees with the conclusion drawn in the Office Action and, pursuant to MPEP § 2144.03, requests that the Examiner provide a specific reference supporting the alleged facts. In the absence of such a specific reference, the Applicant asserts that the Examiner has not met the burden of establishing a *prima facie* case of obviousness.

In addition, the Office Action fails to cite a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art (supported by some reference, and not a mere assertion), to modify any of the cited references in a manner necessary to support the rejection. For this reason, the Applicant urges again that the burden of establishing a *prima facie* case of obviousness has not been met in the Office Action, and requests withdrawal of the Examiner's rejection of Claims 26, 29, 32 and 35-39 under 35 USC § 103(a) as being anticipated by Farrer, Micron, and Wyland. *See*, MPEP § 2143.

Claims 27-28, 30-31, 33 and 34 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al (Farrer) US Patent No. 5,307,320, Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and Wyland US Patent No. 5,261,064 and further in view of Fung et al (Fung) US Patent No. 5,630,163. The Applicant respectfully traverses the Examiner's rejection of these claims.

Considering the arguments set forth by the Applicant previously, and combining the deficiencies in the references noted by the Examiner, the Applicant respectfully urges that this final rejection, attempting to combine the Farrer, Micron, Wyland, and Fung references, fails to provide any motivation to produce a combination which supports a rejection based on obviousness, as required by the M.P.E.P. Merely stating that modification is "within the capabilities of one skilled in the art", or that "those skilled in memory art must be presumed to know something about memory mode apart from what references disclose", and thus, that "it is immaterial that [a] reference does not disclose specific function[s] set forth in Applicant's specification" is logically flawed. Such a statement is tantamount to saying that it doesn't matter what element of an invention is missing from a combination of references - those skilled in the art must have knowledge of the missing element. It is precisely those missing element(s) that make a patentable invention, and thus the Applicant respectfully requests reconsideration by the Examiner with respect to the admitted deficiencies in the references. No evidence whatsoever has been set forth to combine burst EDO memory with the other claimed elements of the invention. As noted above, and pursuant to MPEP § 2144.03, the Applicant requests that the Examiner provide a specific reference supporting the alleged facts. In the absence of such a specific reference, the Applicant asserts that the Examiner has not met the burden of establishing

a *prima facie* case of obviousness, and requests withdrawal of the rejection of claims 27-28, 30-31, 33 and 34 under 35 USC § 103(a) as being anticipated by Farrer, Micron, Wyland, and Fung.

Conclusion

Applicant respectfully submits that all of the pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6904) to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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"Express Mail" mailing label number: EL618436628US
Date of Deposit: June 25, 2001
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box CPA, Washington, D.C. 20231.